The UC4G Wireless MIMO Testbed

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***Abstract*— This paper presents a wireless multiple-input/multiple-output (MIMO) testbed for the UK-China Science Bridges Project: R&D on Beyond Fourth Generation (B4G) Wireless Mobile Communications (UC4G). An introductory review of other approaches is first presented and then subsequently the motivation, architecture and specifications of the UC4G testbed are outlined. The flexibility of operation, versatility of function and modular design of the UC4G testbed are shown to be its key benefits.**

I. Introduction

Channel models and channel measurements in conjunction with system simulations and system metric calculations do offer, to some degree, the possibility of assessing the viability of a novel communications systems, particularly B4G systems. However, they do not offer a complete picture of system performance. Issues such as hardware complexity, transmit and receive synchronization and implementation impairments are not generally addressed by such approaches. For example, in many simulations, only the baseband channel is considered, which in turn could mean that the effect of frequency offset at radio frequency (RF) up-conversion and down-conversion stages may be conveniently ignored. Other aspects of the communications link, such as the quality of the antennas at either end, are also often neglected in this kind of performance assessment. The solution to such analytical shortcomings is to employ a wireless testbed. Here, an introductory review of various testbeds is presented after which the testbed of the UC4G project, referred to hereafter as the UC4G testbed, is discussed.

Testbed designs may be classified as either *link level* or *system level*. Link level testbeds are used to assess single-user point-to-point communication systems whereas system level testbeds consider more than one user and the effect of external interference on a link. For some examples of system level testbeds, the interested reader is referred to [1] and [2]. The discussion here will focus on link level testbeds as these are more relevant to the UC4G testbed.

In [3], the activity of three link level testbeds at University of California, Los Angelos (UCLA) was reported. The first was a non-real time, software-defined, 2×2 MIMO, 5 GHz testbed operating at a bandwidth (BW) of 25 MHz at a maximum transmit power of 18 dBm and was used to demonstrate a combination of MIMO and orthogonal frequency division multiplexing (OFDM), i.e. MIMO-OFDM. The second was a digital signal processing (DSP) based, 3×4 MIMO, testbed operating at a 4 kHz narrow BW in a frequency range of 220 MHz at a maximum Tx power of 35 dBm and was used to demonstrate various space-time block codes, i.e. variations on Alamouti's orthogonal diversity code. Finally, the third was an application specific integrated circuit (ASIC) based, 1×4, 2.4 GHz testbed operating at a BW of 5 MHz at a maximum Tx power of 10 dBm. These three testbeds represent a number of trade-offs in design. The first one offers ease of reconfigurability owing to its software-defined nature but offers little in the way of real-time operation, the second DSP-based testbed offers both a reasonable degree of reconfigurability as well as real-time operation but low data throughput due to the limitations of DSP while the third testbed offers both high throughput and real-time operation because of its ASIC design but requires extensive training and engineering effort in terms of reconfigurability.

At Georgia Institute of Technology (GIT) [4], a PC-based, non-real time, 3×3 MIMO, 2.435 GHz testbed with a BW of 19.53125 MHz was developed and later extended in [5] to a 4×4 MIMO configuration. While the signal processing is software-based and as such could be easily reconfigurable in order to demonstrate or test an arbitrary signal processing technique while providing good data throughput, the emphasis of the work here is purely on the testing of Bell Labs. layered space time (BLAST) OFDM systems.

At the University of A Coruña, the approach is to utilize DSP and field programmable gate array (FPGA) hardware. However these items only appear in the RF chain and as such the baseband signal processing is performed in software on a PC thus allowing a degree of flexibility in this regard. It is a 2×2 MIMO, 2.45 GHz testbed with a receive bandwidth limited to 20 MHz. In [6], a demonstration of Alamouti's code was given with timing and frequency synchronization performed. Furthermore in [7], variations on Alamouti's code, such as differential space-time block codes (STBCs), are also demonstrated and then compared.

There also exist testbeds that operate purely with FPGAs such as the wireless open access research platform (WARP) at Rice University, Texas [8], which notably allows remote access, and also the 4×4 MIMO testbed at the University of Alberta [9]. As well as these, some testbed activities were reported at a recent Globecomm conference [10]. Notable examples include a demonstration of FPGA implementation of

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TABLE I

A SUMMARY OF THE MAIN EXISTING LINK LEVEL PHYSICAL LAYER MIMO TESTBEDS

	BW	MIMO	Architecture	Demo
UCLA(i)	25 MHz	2×2	PC control (non-real time)	MIMO-OFDM
UCLA(ii)	4 kHz	3×4	DSP (real-time)	STBCs
UCLA(iii)	5 MHz	1×4	ASIC (real-time)	Beamforming & Diversity combining
GIT	19.53 MHz	3×3 4×4	PC controlled (non-real time)	BLAST-OFDM
A Coruña	20 MHz	2×2	PC controlled (non-real time)	STBCs
Rice (WARP)	20 MHz	2×2	FPGA (real time)	Various
Alberta	20 MHz	4×4	FPGA (real time)	Channel Measurements
DOCOMO	5 MHz	8×8	FPGA (real time)	ONGO Algorithm

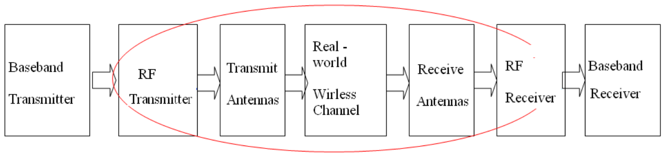

Fig. 1. Descriptive schematic of a wireless testbed.

real-time spatial multiplexing system where the 'DOCOMO' Beijing communications laboratory developed a novel channel estimation algorithm called orthogonal grouping-based near optimal (ONGO) detection for high order, in this case 8×8, MIMO systems [11]. There was also a demonstration of cognitive radio using software defined radio approach to testbed development [12], where a novel algorithm known as Spectrally Modulated Spectrally Encoded (SMSE) was demonstrated.

Another software radio approach is Microsoft Research's, 'software radio', or, 'SORA' [13], where the real-time functioning of the testbed can be controlled by software. A notable achievement of this work was the SISO implementation of the 3GPP long term evolution standard in SORA [14]. A summary of the physical layer link level testbed architectures with MIMO capability is presented in Table I.

While FPGA allows for the design of dedicated MIMO systems that are ready for real-time demonstration and system performance testing, a more ideal solution would be to have both a software-based signal processing interface as well. A key strength of the UC4G testbed is that it facilitates both of these modes of operation. In Section II, the motivation and strengths of the UC4G testbed are discussed. Section III describes the components that comprise the testbed and their operation. Section IV lists the current functionalities of the testbed and provides two sample results. Some concluding remarks are then offered in Section V.

II. MOTIVATION

Fig. 1 presents a descriptive schematic of a generic wireless testbed where it is emphasised that many aspects of communication systems chain such as: up and down conversion processes, antenna gains, and of course the real-world wireless channel are considered. Therefore, testbeds in general are useful for such purposes as: proof-of-concept studies, results calibration, steering of R&D effort, and, indeed, product commercialization. The UC4G project was awarded by the research council UK (RCUK) in 2009 as one of the, 'Science Bridges', projects [15] and funding from the project was used to purchase the UC4G testbed from National Instruments (NI), which was then installed at Heriot-Watt University in Edinburgh, UK.

As mentioned in Section I, the UC4G testbed can facilitate two modes of operation in relation to baseband signal processing. These are referred to as, 'offline', (software-based) and, 'real-time' (FPGA-based). Real-time operation provides a fast and efficient means of obtaining results and a convenient means of demonstrating signal processing systems to an audience. Offline operation is sufficient for all of the aforementioned purposes of a testbed and offers convenient reconfigurability thus making experimentation with various aspects or parameters of signal processing techniques more feasible. This dual operation is one of the main motivations for testbed's acquisition.

The UC4G testbed may be a useful substitute for other types of RF equipment. For example, the FPGA capability of the UC4G testbed can be used in order to develop a device that can mathematically combine a given channel model with baseband data in real-time, i.e., a channel emulator. Also by carefully selecting the type of signal to transmit, say a multi-tone signal, the testbed could also be used to sound the wireless channel for RF channel measurements. The UC4G testbed could therefore be a worthy substitute for other types RF equipment such as channel emulators, channel sounding devices or vector network analyzers, which are, by definition, limited to their specific purpose. Thus, the motivation for the UC4G testbed lies also in its versatility of function.

III. ARCHITECTURE & OPERATION

A photograph of the UC4G testbed may be seen in Fig.2. It consists of 3 major components: a 4-channel transmitter (Tx) chassis on the right and a 2-channel receiver (Rx) chassis on the left. There is also a large hard disk array on the extreme left of the photograph. Each of these components is now introduced.

Fig. 2. Photograph of the UC4G MIMO wireless testbed.

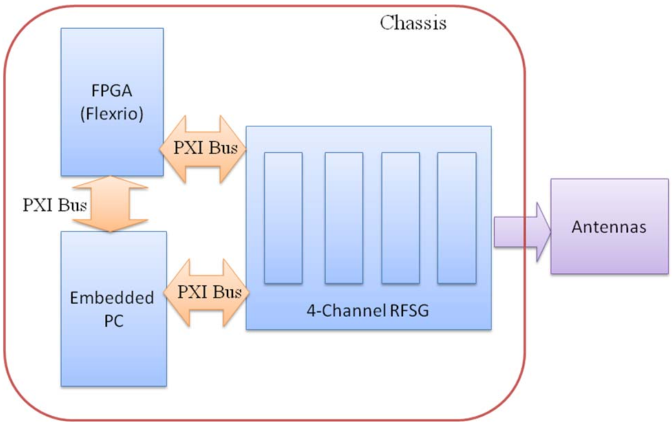

Fig. 3. Tx hardware architecture.

A. Tx Chassis

The transmitter hardware architecture is shown in Fig. 3. It consists of four components: a 4-channel RFSG, a Flexrio FPGA, an embedded PC controller and antennas. These are introduced as follows:

1) 4-channel RFSG: The 4-channel 6.6GHz radio frequency signal generator (RFSG) for signal transmission can be further broken down into several NI devices: a single RF local oscillator (LO), four arbitrary waveform generators (AWGs) and four 6.6GHz RF signal up-converters. The LO generates an RF reference signal and a 10MHz reference clock. Both the RF reference signal and the 10MHz clock are shared by the four RF signal up-converters to enable synchronized transmission. The RFSG has an operational frequency range of 85 MHz to 6.6 GHz and can facilitate a bandwidth of 100 MHz at a max. Tx power of 10 dBm.

2) Embedded PC controller: The embedded PC controller is used to control the Tx and provides networking interfaces. It has an Intel qual-core i7 1.73GHz processor and runs embedded Windows 7 as its operating system. Software that is used to interact with the Tx of the UC4G testbed, i.e. Labview and Matlab, is run from here.

3) NI Flexrio FPGA: The NI Flexrio FPGA board includes a Xilinx Virtex 5 SX 95T FPGA chip and is fully integrated to the PXI backplane. Its primary purpose is to provide real-time signal processing. It possesses 512 MB onboard double data rate (DDR2) dynamic random access memory (DRAM) along with 16 dynamic memory access (DMA) channels for high-speed data streaming at 800 MB/s.

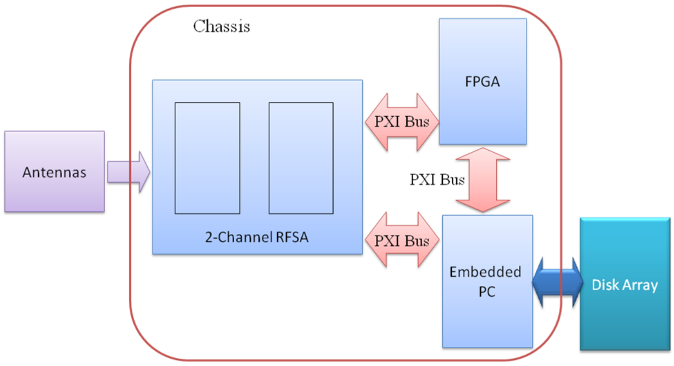

Fig. 4. Rx hardware architecture.

B. Rx Chassis

The receiver hardware architecture is shown in Fig. 4. The receiver has the same 18-slot chassis, embedded PC controller and NI Flexrio FPGA as the transmitter. However, the 4-channel RFSG is replaced with a 2-channel RF signal analyzer (RFSA) at the receiver. In addition, it is also possible to connect a 6 Terabyte (TB) hard drive array, known as a, 'RAID', array to the receiver.

1) 2-Channel RFSA: Similar to the RFSG, the RFSA can be further broken down into several NI modules: one RF local oscillator (LO), two digitizers (ADs) and two 6.6GHz RF signal down-converters. The LO generates an RF reference signal and a 10MHz reference clock. Both the RF reference signal and the 10MHz clock are shared by the two RF signal down-converters to enable synchronized reception. The four digitizers each have an on-board memory of 256M bytes to record RF data. The RFSA can operate in a frequency range of 10 MHz to 6.6 GHz and can facilitate an operational bandwidth of 50 MHz.

2) RAID hard disk array: The redundant array of independent disks or, 'RAID', hard disk array (extreme left of Fig. 2) comprises 12 hard drives giving a total capacity of 6TB. The 12 hard drives work in a multiplexing fashion to allow for a very fast read/write process.

C. Operation

Regardless of whether real-time or offline mode is used, the testbed requires some degree of instrumental control using Labview software. Labview, which is installed on the embedded PCs in either chassis, provides a user-friendly environment for controlling the testbed where the user is easily able to

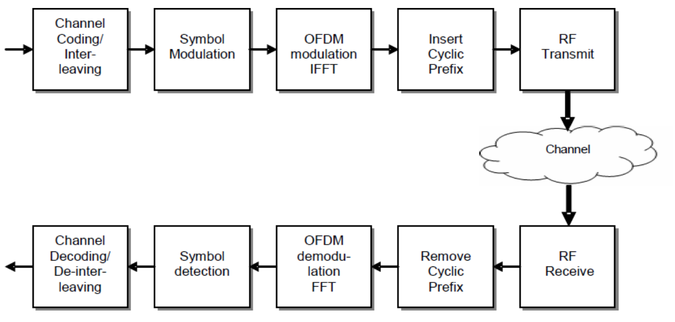

Fig. 5. Schematic of an OFDM system [16].

specify various parameters such as Tx power levels, sample rates, samples to acquire, receiver sensitivity, etc.

IV. Functionality & Results

At present, the UC4G testbed can demonstrate the following functionalities:

- Spatial modulation (offline) [17].
- MIMO LTE (offline).
- Channel emulation (FPGA).
- Channel measurement.
- SISO OFDM (real-time FPGA).

Testbed development results for the SISO OFDM, MIMO LTE, and channel emulation are now presented.

A. SISO OFDM

OFDM Tx and Rx signal processing architectures have been developed in Labview FPGA for the case of a SISO link. The block diagram for the OFDM system is pictured in Fig. 5 The input bits are mapped onto symbol sequences and are then assigned subcarriers. Pilot sequences are then generated to estimate the channel and a guard bit ensures robust OFDM symbol transmission. An inverse fast Fourier transform (IFFT) is then applied to the sequence where typically a cyclical prefix is also used to ensure circular convolution with the channel. These processes are then reversed at the Rx end to recover the original bit sequence.

The system runs in real-time and a constellation diagram appears showing the demodulated QAM symbols. The user can, for example, block or move the antenna into a different polarisation state and observe in real-time the effect on the constellation diagram and hence on system performance. Fig.6 shows a 16 QAM constellation diagram and the parameters of this system are: Bandwidth: 20 MHz; Carrier frequency 2.3 GHz; spacing at transmit and receive antennas: $\lambda/2$; Receiver reference level: -30 dBm. The testing environment was fixed position, line-of-sight (LOS) in a furnished laboratory.

B. MIMO LTE

At the Vienna University of Technology, a MIMO link-level LTE simulator was developed as an open source project in order to encourage reproducibility in terms of testing MIMO algorithms [19]. The project is based on the MIMO LTE

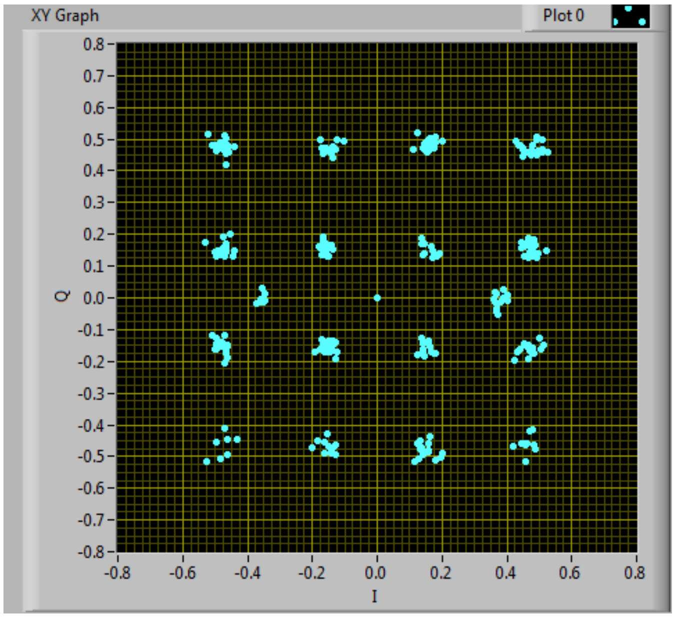

Fig. 6. 16 QAM constellation of an OFDM system implemented on the UC4G testbed in real-time FPGA.

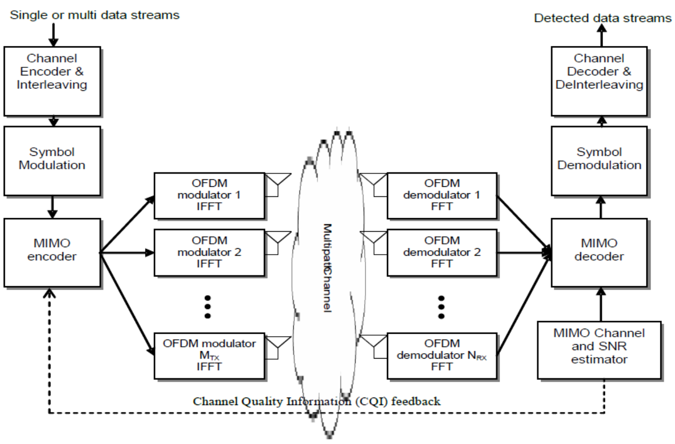

Fig. 7. Schematic of the MIMO LTE standard [16].

standard [18] and comprises OFDM signals in combination with various MIMO schemes. An overview of the MIMO LTE system is given in Fig.7.

Specifically, it is possible to consider three modes of MIMO operation: (i) Transmission diversity (TxD); (ii) open-loop spatial multiplexing; and (iii) closed-loop spatial multiplexing. The choice of operation scheme depends on the quality of the channel and is decided by feedback of the channel quality indicator (CQI) to the transmitter. In these demonstrations, no feedback path is available thus transmit diversity and open-loop spatial multiplexing (hereafter, 'multiplexing'), are tested separately and compared. In both cases, the entire 4×2 set of RF chains on the testbed is used. The operational modes of multiplexing and diversity are compared in Fig.8

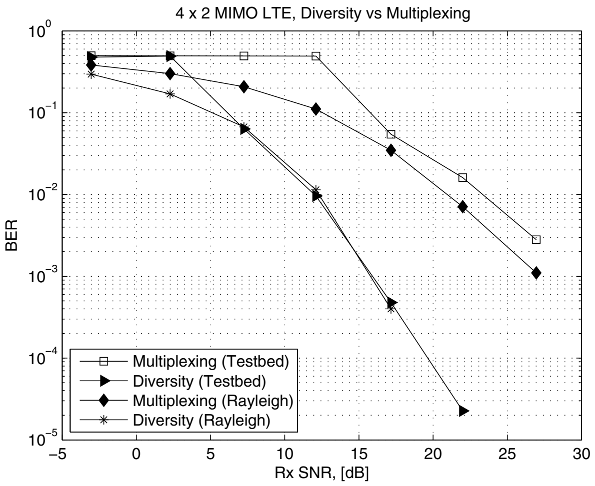

Fig. 8. Comparison of BERs for MIMO LTE diversity and multiplexing.

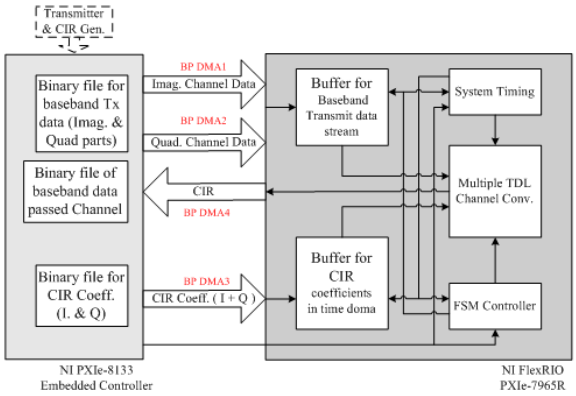

Fig. 9. Schematic of channel emulator architecture.

TABLE II

COMPARISON OF RUN TIME FOR CHANNEL EMULATOR VS SOFTWARE APPLYING C4 WINNER II CHANNEL MODELS.

LTE Baseband data	**Channel simulator**	**Channel emulator**
26 MSamples	159.097s	14.682s

and the parameters of the system are: 16 QAM modulation; Bandwidth: 20 MHz; carrier frequency 2.3 GHz; Spacing at transmit and receive antennas: $\lambda/2$. The testing environment was fixed position, LOS in a furnished laboratory.

The diversity scheme exhibits better BER performance than the multiplexing one, which is reasonable since diversity is inherently more reliable. The testbed results are compared with a simulation over Rayleigh channels. For case of diversity, the match is exact however for multiplexing, the testbed channels performed worse than the Rayleigh channels. This is to be expected since the testbed is operating in LOS channels and thus cannot fully facilitate multiplexing due to the ill-conditioned channels that would arise in this case.

C. Channel emulation

The concept of channel emulation is that of being able to take an arbitrary channel model and convolve this channel with transmit data, thus emulating, a desired channel. The main advantage over software approaches is the higher speed of such a device. Like the OFDM system described in Section IV-A, the channel emulator will make use of the FPGA board in the testbed chassis. The architecture for the device is shown in Fig. 9.

In the testbed, the PC reads the data from a local hard drive, in which the in-phase and quadrature (IQ) components of baseband modulated signals and the channel impulse response coefficients are stored. Then, these data are passed through dynamic memory access channels (DMA) channels to an FPGA module (Xilinx Vertex 5-ST95). There are 4 parallel distinct DMA channels available between the embedded controller and the NI FlexRIO FPGA module. As shown in Fig. 9, the IQ baseband data and the channel impulse response (CIR) coefficients are fed into the FPGA module via DMA channel 1, 2 and 3, respectively. The baseband signal passes through the emulated channel then back to the embedded controller via backplane (BP) DMA channel 4.

Once the data has been combined correctly, convolution between the CIR and the baseband IQ data is performed. The hardware architecture design for the channel convolution module is completed in FPGA with LabVIEW FPGA tools. This mathematical function consists of the following functional operations:

- Shift registers: These are used to store and shift the IQ baseband samples (acting as tap delays) and channel coefficients.
- Control logic to load channel coefficients: The IQ channel coefficients are transferred into FPGA serially via one DMA channel. This control logic is in charge of serial to parallel conversion and loading the whole chunk of channel coefficients into multipliers regularly.
- Multipliers: These are implemented to complete the complex multiplication of baseband signals and channel coefficients.
- Adders: The pipelined adders are to improve the processing clock rate.

In order to assess the channel emulator's performance, its run time is compared with that of software. The software in question is Matlab 2011 running on a windows Windows 7 machine with Intel Core i7 1.73GHz and 4GB RAM. In both cases some LTE baseband transmit data is being convolved with a C4 WINNER II channel model. The simulation times are compared in Table. II

It is clear that the channel emulator is over 10 times faster than the software-based channel simulator and thus there is a clear advantage to the development of a channel emulator based on the UC4G testbed.

V. Conclusions

In this paper, an introductory review of testbeds has been first presented along with motivation, architecture, operation, functionality and results from the UC4G testbed. The key benefit of the UC4G testbed is that it combines the convenience of having both real-time (FPGA based) operation and flexible offline (software) operation with versatility of function. Results from three UC4G testbed implementations have been presented, namely a real-time implementation of OFDM, an offline implementation of MIMO LTE and channel emulation. The future outlook is to exploit the modular design of the UC4G testbed by increasing the amount of RF modules in order to test duplex systems. Key B4G technologies in this regard include cooperative MIMO systems [20], [21], cognitive radio [22] and vehicular communication systems [23], [24].

Acknowledgments

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